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SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

1.Field of the Invention

The present invention relates to a semiconductor device and a method for manufacturing the semiconductor device, particularly to technique improving withstanding operating voltage while depressing decrease of driving ability.

2.Description of the Related Art

Fig. 5 is a sectional view describing the conventional semiconductor device.

In Fig. 5, symbol 51 is first conductive, for example P type, semiconductor substrate, on the substrate 51, a gate electrode 53 is formed through a gate oxide film 52, and a source-drain region of one side LDD (Lightly Doped Drain) structure is formed so as to be adjacent to the gate electrode 53. That is a semiconductor device having a source-drain region of one side LDD structure in which high concentration (N+ type) source region 55 is formed at source region side so as to be adjacent to said gate electrode 53, low concentration (N- type) drain region 54 is formed at drain region side so as to be adjacent to said gate electrode 53, and high concentration (N+ type) drain region 56 is formed in the low concentration

drain region 54.

As described above, in the semiconductor device of one side LDD structure in which high voltage is applied only to drain region side, high concentration drain region 56 is surrounded with low concentration drain region 54 to defuse concentration of electric field in drain region side as above-mentioned. However, in source region side, only high concentration source region 55 exists.

Even the semiconductor device having such the structure is needless to take its structure as a particular problem with regard to static withstanding voltage. However, at operation, the following problem occurs.

That is, in a bipolar structure consisting of a source region (emitter region), a substrate (base region), and a drain region (collector region), injection efficiency of carrier is good because high concentration source region 55 is exposed in emitter region, so that the bipolar transistor is made on easily by a little substrate current Isub.

That is, since current gain β in the bipolar transistor is high, drain withstanding voltage at operation decreases comparing with semiconductor of both sides LDD structure.

Here, in order to improve drain withstanding voltage at operation, it needs to decrease substrate current Isub. That is, it needs to make further drain electric field weak.

However, when impurity concentration of whole low

concentration drain region 54 is made thin in order to decrease substrate current Isub, the substrate current Isub has double hump structure having two peaks ((1) and (2)) as voltage Vg increases as shown in Fig. 6.

When the low concentration drain region 54 is further low, the first peak (1) of the substrate current Isub is low so that drain withstanding voltage at low Vgs improves. However, the second peak (2) of the substrate current Isub is comparatively high so that drain withstanding voltage at high Vgs decreases.

Conversely, when whole impurity concentration of the low concentration drain region 54 is high, one peak having a certain voltage Vgs appears so as to be useful for drain withstanding voltage at high Vgs decreases as shown in Fig. 6. However, there is a problem that drain withstanding voltage at low Vgs can not withstand.

Thus, when whole impurity concentration of the low concentration drain region 54 is changed uniformly, the change can not get out of the trade-off relation of drain withstanding voltage at low Vgs and drain withstanding voltage at high Vgs.

Although current gain β decreases and withstanding voltage withstands decidedly by adopting both sides LDD structure generally used, the device has distance (L) of drift region similar as drain side shown in Fig. 5, so that on-resistance increases and driving ability decreases because usual LDD structure is adopted at source side in spite of no need of

withstanding voltage at source side.

SUMMARY OF THE INVENTION

The invention carried out in view of the above-mentioned problems is a semiconductor device comprising: a gate electrode formed on a first conductive type semiconductor substrate via a gate oxide film; a first low concentration drain region of a second conductive type, being formed adjacent to one end of said gate electrode; a second low concentration drain region of the second conductive type, being formed in said first low concentration drain region so that said second low concentration drain region is very close to the outer boundary of said first low concentration drain region, and being higher in impurity concentration than at least impurity concentration of the first low concentration drain region; and a high concentration source region of the second conductive type being formed adjacent to another end of said gate electrode and a high concentration drain region of the second conductive type being formed in said low concentration drain region having a predetermined distance from the one end of said gate electrode.

A method for manufacturing a semiconductor device comprises: a first process comprising steps of a first step forming a first photo resist film having a first opening at a drain forming region on a first conductive type semiconductor substrate, a second step ion-implanting a first impurity of

the second conductive type and a second impurity of the second conductive type with the first photo resist film being used as a mask, and a third step forming a first low concentration drain region of the second conductive type and a second low concentration drain region of second type by diffusing said first impurity and said second impurity after the fore-mentioned ion-implanting step; a second process forming an element separation film at a predetermined region by selectively oxidizing with an oxidization resist film formed on said substrate as a mask and forming a second gate oxide film at region except the element separation film and the first gate oxide film; a third process forming a gate electrode so as to cover from said first gate oxide film to the second gate oxide film; a fourth process forming a second photo resist film having a second opening on the source forming region on said substrate and having a third opening on a region separated from another end of said gate electrode on said low concentration drain region; and a fifth process forming high concentration source-drain regions of the second conductive type by ion-implanting a third impurity of the second conductive type on said substrate with said second photo resist film, said gate electrode, said element separation film, and said first gate oxide film as a mask.

Thus, the second low concentration drain region higher in impurity concentration than impurity of the first low

concentration drain region is formed in said first low concentration drain region of second conductive type so that said second low concentration drain region is very close to the outer boundary of said first low concentration drain region. By that, the low concentration drain region is made with a double structure consisting of two kinds of impurity ions different in diffusion coefficient without uniformly changing impurity distribution in the low concentration drain region. Therefore, the first low concentration drain region withstands low Vgs withstanding voltage, and the second low concentration drain region withstands high Vgs withstanding voltage.

Further, the process forming said first low concentration drain region and second low concentration drain region have a process thermal-treating, at the same time, said first impurity consisting of phosphorus ion and said second impurity consisting of arsenic ion and use difference of diffusion coefficients of these impurities.

Thus, since difference of diffusion coefficients of two kinds of impurities is used and these impurities are formed at the same process when the first low concentration drain region and the second low concentration drain region are formed, the second low concentration drain region can be formed accurately at very near part in the first low concentration drain region.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a sectional view showing a method for manufacturing a semiconductor device according to the mode for carrying out the invention.

Fig. 2 is a sectional view showing a method for manufacturing a semiconductor device according to the mode for carrying out the invention.

Fig. 3 is a sectional view showing a method for manufacturing a semiconductor device according to the mode for carrying out the invention.

Fig. 4 is a sectional view showing a method for manufacturing a semiconductor device according to the mode for carrying out the invention.

Fig. 5 is a sectional view showing the conventional semiconductor device.

Fig. 6 is a view describing the conventional problem.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

An embodiment of a semiconductor device of the present invention and a method for manufacturing the semiconductor device according to the present invention will be described referring figures.

In the semiconductor device according to the invention, a gate electrode 9 is formed on P type, for example, semiconductor substrate 1 so as to cover from a first gate oxide film 7A

to a second gate oxide film 8 as shown in Fig. 4.

A high concentration (N+ type) source region 10 is formed so as to be adjacent to one end of said gate electrode 9 (one end of the second gate oxide film 8). Further, a first low concentration (LN type) drain region 5 is formed so as to be adjacent to the other end of said gate electrode 9 (the other end of the first gate oxide film 7A), and a second low concentration (SLN type) drain region 6 at least higher in impurity concentration than impurity of the first low concentration (LN type) drain region 5 is formed in the first low concentration (LN type) drain region 5 so that the second low concentration drain region 6 is very close to the outer boundary of the first low concentration drain region 5. Further in the drain region 6, high concentration (N+ type) drain region 11 is formed at region separated from said gate electrode 9 (so as to be adjacent to one end of said first gate oxide film 7A).

Adopting such the construction, the second low concentration (SLN type) drain region 6 higher in impurity concentration than impurity of the first low concentration (LN type) drain region 5 is formed in said first low concentration (LN type) drain region so that said second low concentration drain region 6 is very close to the outer boundary of said first low concentration drain region 5. By that, low concentration drain region is made with a double structure consisting of two kinds of impurity ions different in diffusion

coefficient, that is, covering thinly the second low concentration (SLN type) drain region 6 higher in impurity concentration than impurity of the first low concentration (LN type) drain region 5 with the first low concentration (LN type) drain region 5, without changing uniformly impurity distribution in the low concentration drain region conventionally. Therefore, the first low concentration (LN type) drain region 5 withstands low Vgs withstanding voltage, and the second low concentration (SLN type) drain region 6 withstands high Vgs withstanding voltage so as to improve drain withstanding voltage at operation.

Thus, by construction that the low concentration drain region has two or more kinds of different impurity concentrations, and not by changing impurity distribution uniformly over whole low concentration drain regions, drain withstanding voltage at operation can be improved with independence of trade-off relation of drain withstanding voltage at low Vgs and drain withstanding voltage at high Vgs.

Since it is needless to adopt the conventional semiconductor device of LDD structure having substantially symmetry low concentration source-drain regions in source-drain regions and the device according to the invention does not have drift region comparing with the conventional semiconductor device, decrease of the driving ability can be depressed.

A method for manufacturing the above-mentioned

semiconductor device will be described below referring the figure.

First, in Fig. 1, a photo resist (PR) film 2 having an opening on a drain forming region on a P type semiconductor substrate 1 is formed, with using the photo resist (PR) film 2 as a mask, and first and second impurity implantation regions are formed by ion-implanting first and second impurities. At this time, said second impurity is required to be an impurity less in diffusion coefficient than said first impurity, and when said first impurity is phosphorus-ion, arsenic-ion, for example, is used for the second impurity. After a first impurity implantation region 3 is formed by ion-implanting phosphorus-ion with acceleration voltage of 100 KeV and dose of about 6 x $10^{12}/cm^2$, a second impurity region 4 is formed by ion-implanting arsenic-ion with acceleration voltage of 160 KeV and dose of about 5 x $10^{11}/cm^2$.

Next, in Fig. 2, after removing said photo resist film 2, a first low concentration (LN type) drain region 5 is formed by thermal-diffusing said phosphorus ion and arsenic ion, and a second low concentration (SLN) drain region 6 higher in impurity concentration than at least low concentration drain region 5 is formed in the low concentration drain region so that the second low concentration drain region 6 is very close to the outer boundary of the first low concentration drain region 5. At this time, thermal treatment of about 1100 ℃ and 4 hours

is carried out in this embodiment.

In the process, two kinds of impurity ions (phosphorus ion and arsenic ion) different in diffusion coefficient are ion-implanted using the same mask (photo resist film 2) and diffused using difference of diffusion coefficients of these impurities. Because of that, the second low concentration (SLN type) drain region 6 comparatively high in impurity concentration can be formed so as to be covered with thin first low concentration (LN type) drain region 5 with suitable space.

Next, in Fig. 3, after forming a pad oxide film and a silicon nitride film as oxidation resistance film having an opening at the designated region (first gate oxide film forming region and element separation film forming region) not shown on said substrate 1, a first gate oxide film 7A and an element separation film 7B of about 1000 nm thickness are formed using the silicon nitride film as a mask and oxidizing selectively by known LOCOS method. Further after removing said pad oxide film and silicon nitride film, a second gate oxide film 8 of 150 nm thickness is formed by thermal-oxidizing on the substrate where said first gate oxide film 7A and element separation film 7B are not formed. Then, after a polysilicon film of 400 nm thickness is formed on said substrate 1 and carrying out conducting treatment of the polysilicon film, a gate electrode 9 is formed so as to cover from said first gate oxide film 7A to the second gate oxide film 8 patterning a photo resist

film not shown used as a mask. At this time, the second gate oxide film 8 on the substrate 1 except the part where the gate oxide film 8 is formed is removed.

Further, in Fig. 4, N type impurity is ion-implanted so as to be adjacent to one end of said gate electrode 9 using a photo resist (PR) film 12 formed on said substrate 1 as a mask. Ion-implanting N type impurity so as to separate from the other end of said gate electrode 9 and to be adjacent to one end of said gate oxide film 7A, a high concentration (N+ type) source region 10 is formed so as to be adjacent to one end of said gate electrode. Then, a high concentration (N+ type) drain region 11 is formed at a region separated from the other end of said gate electrode 9 (so as to be adjacent to the other end of said first gate oxide film 7A) in said second low concentration drain region 6. At this time, arsenic ion is ion-implanted with acceleration voltage of about 80 KeV and implanting quantity of about 6 X $10^{15}/cm^2$.

Although description shown in the figure is omitted, source-drain electrodes are formed through contact holes after forming insulation film between layers over whole surface forming the contact holes on the insulation film between layers so as to contact to said source-contact regions.

Thus, in the method for manufacturing the semiconductor device of the present invention, two kinds of impurities (phosphorus ion and arsenic ion) which are ion-implanted

previously on surface of said substrate and are different in diffusion coefficients are treated with thermal diffusion. Using the difference of the diffusion coefficients, a low concentration drain region of double structure having two kinds of impurity concentration is formed. That is, the low concentration drain region is formed so as to cover thinly the second low concentration (SLN type) drain region 6 (based on arsenic ion) with the first low concentration (LN type) drain region 5 (based on phosphorus ion). Therefore, differing from changing impurity concentration uniformly over whole low concentration drain regions as conventionally, drain withstanding voltage at operation can be improved with independence of trade-off relation of drain withstanding voltage at low Vgs and drain withstanding voltage at high Vgs.

According to the invention, by forming a low concentration drain region so as to have two kinds of different impurity concentration, low Vgs withstanding voltage withstands at a first low concentration drain region low in impurity concentration withstands, and high Vgs withstanding voltage withstands at a second low concentration drain region high so as to improve drain withstanding voltage at operation.

Because the first low concentration drain region and the second low concentration drain region are formed using difference of the diffusion coefficients by thermal treatment of two kinds of impurities which are previously ion-implanted to surface

of a substrate and are different in diffusion coefficient, the second low concentration drain can be formed in the first low concentration drain region so that said second low concentration drain is very close to the outer boundary of said first low concentration drain region.